CLAIMS

1. An apparatus comprising:

a first circuit configured to (i) select one of a plurality of input signals and (ii) generate (a) an output signal having a frequency and (b) one or more control signals in response to a skew signal; and

a second circuit configured to generate said skew signal in response to said one or more control signals, wherein said first circuit is configured to minimize skew between said selected input signal and a feedback of said output signal in response to said skew signal.

2. The apparatus according to claim 1, wherein said first circuit further comprises:

a digitally programmable delay circuit configured to delay said selected input signal and said feedback of said output signal.

3. The apparatus according to claim 2, wherein said digitally programmable delay circuit is configured to independently

delay said selected input signal and said feedback of said output signal.

4. The apparatus according to claim 1, wherein said second circuit comprises:

a counter circuit configured to generate said skew signal in response to said one or more control signals, wherein said skew signal comprises a digital word.

5. The apparatus according to claim 1, wherein said first circuit further comprises a phase locked loop (PLL) configured to generate said output signal.

6. The apparatus according to claim 1, wherein said selected input signal comprises a reference clock signal.

7. The apparatus according to claim 1, wherein said first circuit comprises:

a plurality of phase comparators configured to generate said plurality of control signals.

8. The apparatus according to claim 1, wherein said apparatus comprises a digitally based skew and low frequency phase noise reduction circuit.

9. The apparatus according to claim 1, wherein said apparatus is implemented externally to an existing PLL.

10. The apparatus according to claim 1, wherein said apparatus is configured to provide a self test of an internal skew.

11. The apparatus according to claim 1, wherein said first circuit comprises:

a phase comparator circuit configured to receive said plurality of input signals and generate said one or more control signals;

a multiplexer circuit configured to receive said one or more control signals and generate a first clock signal and a second clock signal; and

a delay circuit configured to delay said first and second clock signal in response to said skew signal.

12. The apparatus according to claim 1, wherein said second circuit comprises:

a multiplexer circuit configured to receive said one or more control signals; and

a counter circuit configured to receive an output of said multiplexer and generate said skew signal.

13. The apparatus according to claim 1, wherein said one of said input signals is hardwired to said first circuit and said output signal is hardwired to said first circuit.

14. An apparatus comprising:

means for (i) generating (a) an output signal having a frequency and (b) one or more control signals in response to a skew signal and (ii) selecting one of a plurality of input signals;

means for generating said skew signal in response to said one or more control signals; and

means for minimizing timing skew between said selected input signal and a feedback of said output signal.

15. A method for correcting skew between an input signal and a feedback of an output signal, comprising the steps of:

(A) receiving a plurality of input signals;

(B) selecting one of said plurality of input signals;

(C) generating a skew signal in response to said selected input signal and a feedback of said output signal; and

(D) adjusting a delay between said selected input signal and said feedback of said output signal, in response to said skew signal.

16. The method according to claim 15, wherein step (D) further comprises:

digitally programing said delay.

17. The method according to claim 15, wherein said skew signal comprises a digital word.